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Claims

[c1] A method of forming bitlines for a memory cell array of an integrated circuit and conductive lines interconnecting transistors of an external region outside of said memory cell array, comprising:
patterning troughs in a dielectric region covering said memory cell array according to a first critical dimension mask only;
forming bitline contacts to a substrate and bitlines in said troughs; and
forming conductive lines consisting essentially of at least one material selected from the group consisting of metals and conductive compounds of metals in horizontally oriented patterns patterned by a second critical dimension mask, said conductive lines interconnecting said bitlines to transistors of external circuitry outside of said memory cell array, said conductive lines being interconnected to said bitlines only at peripheral edges of said memory cell array.

[c2] The method of claim 1 wherein said bitline contacts are formed borderlessly to wordlines coupled to said memory cell array, said wordlines being encapsulated by in-

sulative material.

[c3] The method of claim 1, wherein said bitline contacts include a first layer consisting essentially of polysilicon and said bitlines include a second layer consisting essentially of at least one material selected from the group consisting of metals and conductive compounds of metals.

[c4] The method of claim 3 wherein said second layer is formed by etching back said first layer in said troughs and then simultaneously depositing said at least one material selected from the group consisting of metals and conductive compounds of metals while depositing said at least one material in said horizontally oriented patterns to form said conductive lines.

[c5] The method of claim 2 wherein said bitlines and said bitline contacts consist essentially of at least one material selected from the group consisting of metals and conductive compounds of metals.

[c6] The method of claim 5 wherein said first critical dimension mask includes elongated line-space patterns such that said troughs extend linearly across a multiplicity of said encapsulated wordlines.

[c7] The method of claim 6 wherein said conductive lines are

broader than said bitlines where said conductive lines interconnect to said bitlines.

[c8] The method of claim 7 wherein said conductive lines interconnect pairs of said bitlines to sense amplifiers located in said external regions beyond opposite edges of said memory cell array, wherein successive pairs of said bitlines are coupled to sense amplifiers located in alternating ones of said external regions.

[c9] The method of claim 8 wherein said interconnections between said conductive lines and said bitlines are formed over isolation structures substantially unaffected by patterning of said troughs and said horizontally extending patterns.

[c10] The method of claim 1 further comprising forming vertically extending patterns in said external region prior to forming said horizontally extending patterns, at least some of said vertically extending patterns contacting said substrate, and simultaneously filling said troughs, said vertically extending patterns and said horizontally extending patterns to form conductive contacts and said conductive lines.

[c11] A method of forming contacts to a substrate of an integrated circuit (IC) for an array of memory cells and for

external circuitry outside of said array, comprising:
forming an array of memory cells in an array portion of a substrate, each cell including a storage capacitor and an array transistor;
forming encapsulated wordlines for operating said memory cells;
forming external transistors in an external portion of said substrate outside of said array portion;
forming a dielectric layer covering said array of memory cells and said external transistors;
forming troughs in said dielectric layer in said array portion; said troughs running in a direction transverse to said wordlines;
forming array contacts in said troughs, said array contacts extending to said substrate;
forming bitlines in said troughs above said array contacts, said bitlines including at least one material selected from the group consisting of metals and conductive compounds of metals;
forming external contacts to said substrate in said external portion of said substrate; and
simultaneously forming conductive interconnects between ones of said external transistors and between said bitlines and said external transistors;
forming a conductor layer in said troughs including a material selected from the group consisting of metals

and conductive compounds of metals;
forming external contacts to said single-crystal semiconductor in said external region; and
simultaneously forming conductive interconnects between ones of said external transistors and between said conductor layer and said external transistors.

[c12] An integrated circuit including a memory cell array and an external region outside of said memory cell array, comprising:
bitline contacts to a substrate and bitlines disposed in said memory cell array; and
metallic conductive lines interconnecting said bitlines to transistors disposed in said external region, said conductive lines being patterned separately from said bitlines.

[c13] The integrated circuit of claim 12 wherein said bitline contacts and said bitlines are disposed in troughs formed in a dielectric region, each said trough having a pair of vertical sidewalls, each said sidewall extending substantially in a single plane between said conductive lines and said substrate.

[c14] The integrated circuit of claim 13 further comprising conductive interconnections interconnecting said bitlines to said external transistors, said conductive interconnec-

tions being patterned simultaneously with said conductive lines.

[c15] The integrated circuit of claim 14 further comprising wordlines encapsulated by insulative material, wherein said bitline contacts include borderless contacts disposed between said encapsulated wordlines.

[c16] The integrated circuit of claim 15 wherein said bitline contacts include at least a first layer consisting essentially of polysilicon and said bitlines include at least a second layer consisting essentially of at least one material selected from the group consisting of metals and conductive compounds of metals.

[c17] The integrated circuit of claim 15 wherein said bitlines and said bitline contacts consist essentially of at least one material selected from the group consisting of metals and conductive compounds of metals.

[c18] The integrated circuit of claim 17 wherein said conductive lines are broader than said bitlines where said conductive lines interconnect to said bitlines.

[c19] The integrated circuit of claim 18 wherein said conductive lines interconnect pairs of said bitlines to sense amplifiers located in said external regions beyond opposite edges of said memory cell array, wherein successive

pairs of said bitlines are coupled to sense amplifiers located in alternating ones of said external regions.

[c20] The integrated circuit of claim 19 wherein said interconnections between said conductive lines and said bitlines are disposed over isolation structures, said isolation structures isolating said substrate from said bitlines and said conductive lines.